Main functions and rated parameters:

- 600V/20AThree Phase DC to AC Inverter
- Built-in Low Loss Trench Gate-Field Stop TypeIGBT
- lower armIGBTemitter output
- Built-in bootstrap diode

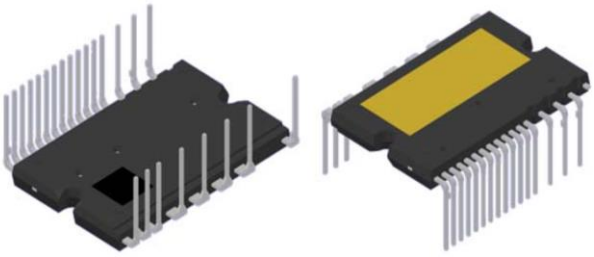
application

- Air-conditioning compressor
- refrigerator compressor
- low power inverter
- industrial sewing machine

Features:

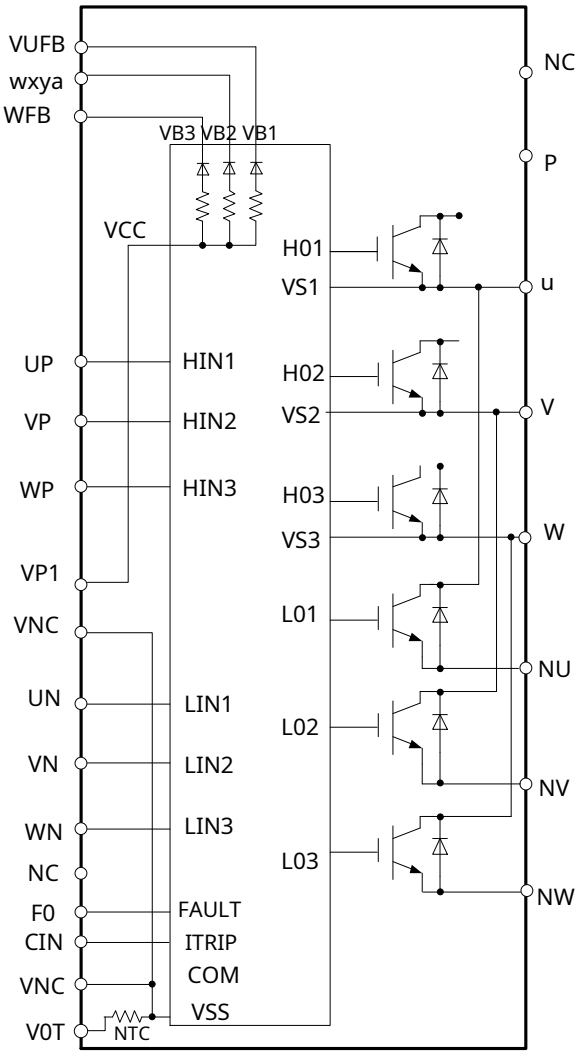
- IGBTDrive: Enhanced input filtering, upper and lower arm interlock, high speed600VLevel conversion, power supply undervoltage protection, short circuit (overcurrent) protection.
- Fault signal: corresponding to short circuit (overcurrent) andVP1power supply Undervoltage fault.
- Input Interface: Compatible3.3V&5VInput signal, active high.
- Temperature detection: Negative temperature coefficient thermistor detection output.

Package form



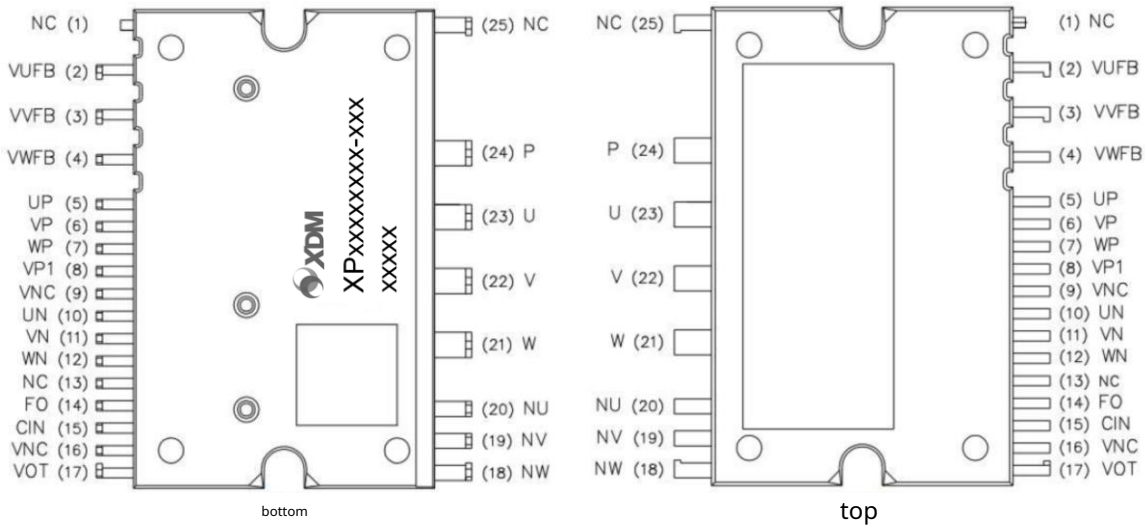
product name	Package form	print name
XP20G60AS0-CJC	DIP25-CU	XP20G60AS0-CJC

Module internal circuit diagram



picture1: Internal circuit diagram

Pin description



picture2: pin diagram

Pin No.	Pin name	Pin Description
1	NC	no connection
2	VUFB	uPhase upper arm drive power terminal
3	wxya	VPhase upper arm drive power terminal
4	WFB	WPhase upper arm drive power terminal
5	UP	uPhase upper arm control signal input terminal
6	VP	VPhase upper arm control signal input terminal
7	WP	WPhase upper arm control signal input terminal
8	VP1	Control power terminal
9	VNC	control powerGNDterminal
10	UN	uPhase lower arm control signal input terminal
11	VN	VPhase lower arm control signal input terminal
12	WN	WPhase lower arm control signal input terminal
13	NC	no connection
14	FO	Fault output terminal
15	CIN	Short circuit protection trigger voltage detection terminal
16	VNC	control powerGNDterminal
17	VOT	Temperature detection output terminal
18	NW	Wlower armIGBTemitter terminal
19	NV	Vlower armIGBTemitter terminal
20	NU	ulower armIGBTemitter terminal
twenty one	W	WPhase output terminal
twenty two	V	VPhase output terminal

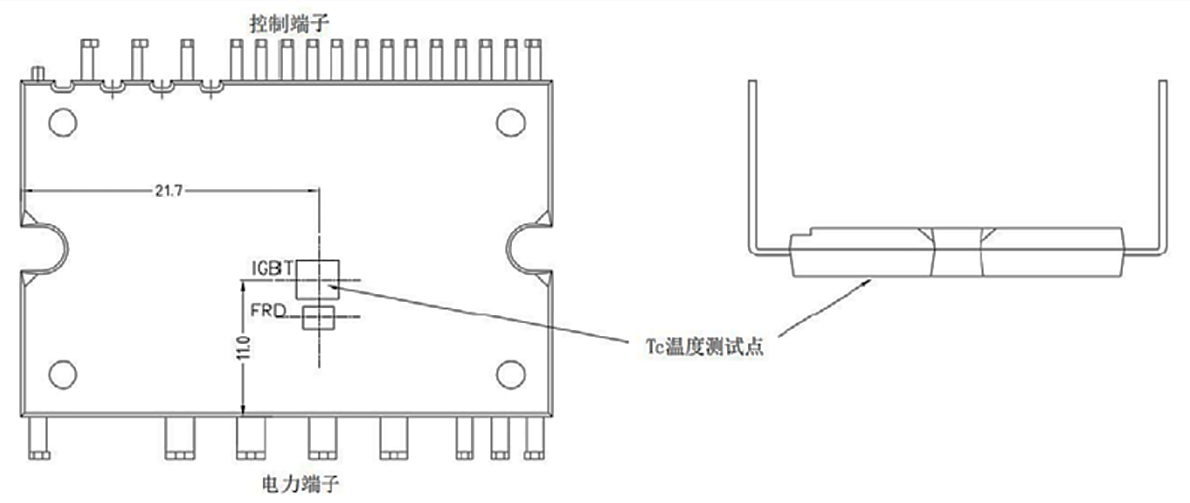
twenty three	u	uPhase output terminal
twenty four	P	Inverter DC input terminal
25	NC	no connection

Maximum Ratings (Tj= 25°C,unless otherwise specified)

mark	project	condition	rated value	unit
inverter part				
V_{CC}	voltage	apply toP-NU,NV,NWbetween	450	V
V_{CC} (Surge)	Power supply voltage (including surge)	apply toP-NU,NV,NWbetween	500	V
V_{CES}	Collector-emitter voltage		600	V
±I_C	collector current	T_C=25°C (TcThe test method is shown in the figure3)	20	A
±I_{CP}	Collector current (peak value)	T_C=25°C,Pulse width less than1ms	40	A
P_C	collector power consumption	T_C=25°C,single chip	50	W
Tj	junction temperature	(see note1)	- 55~+175	°C
Control section				
V_{DB}	High side control supply voltage	apply toUFB-U, VFB-V, WFB-Wbetween	17.5	V
$V_{D.}$	Control supply voltage	apply toVP1–VNCbetween	17.5	V
V_{IN}	input signal voltage	apply toUP,VP,WP,UN,VN,WN–VNCbetween	- 1~10	V
V_{FO}	Fault output voltage	apply toFO–V_{NC}between	- 0.5~VD+0.5	V
I_{FO}	Fault output current	FOTerminal sink current value	1.5	mA
V_{SC}	Current detection terminal input voltage	apply toCIN–V_{NC}between	- 0.5~VD+0.5	V
system-wide				
$V_{CC(PROT)}$	Power supply voltage self-protection range (short circuit)	$V_{D.}$=V_{DB}=13.5~16.5V Tj=150°C,no repeat, time less than2us	400	V
Tc	Normal working case temperature of the module	- 20°C≤Tj≤150°C	- 20~100	°C
Tstg	Storage temperature		- 55~125	°C
Viso	Dielectric withstand voltage	sine wave60Hz, AC1min, between pin and heat sink	2500	Vrms

Remark1: IPMThe maximum rated junction temperature of the power chip is175°C (@surface temperatureT_C≤ 100°C). However, to ensureIPMFor safe operation, the junction temperature should be limited to$T_{j(av)}$ ≤

150°C (@surface temperatureTc ≤ 100°C).



picture3: Shell temperature test point

thermal resistance

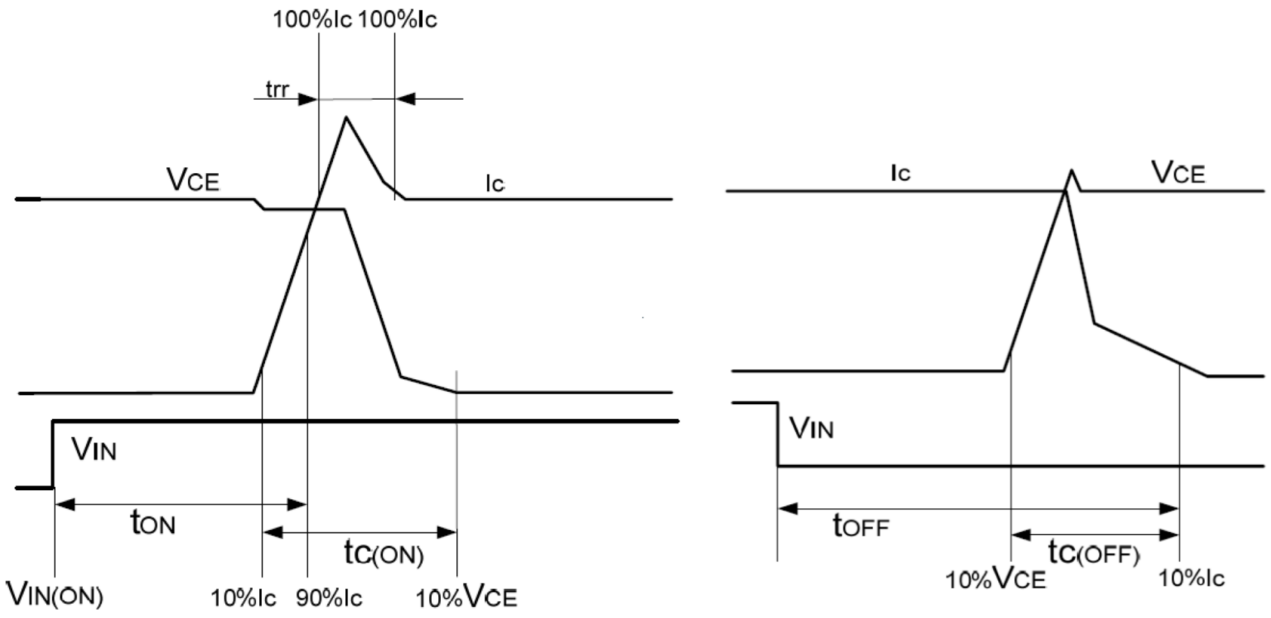
mark	project	condition	minimum value	typical value	maximum value	unit
Rth(jc)Q	Junction to Case Thermal Resistance	singleIGBTelement	-	-	2.5	°C/W
Rth(jc)F		singleFRDelement	-	-	3.4	°C/W

electrical characteristics(Tj= 25°C,unless otherwise specified)

inverter part

mark	project	condition	minimum value	typical value	maximum value	unit
$V_{CE(sat)}$	Saturation voltage between collector and emitter	$V_{D.}=V_{DB}=15V$ $V_{IN}=5V$, $I_C=20A,T_j=25°C$	-	1.65	1.95	V
		$V_{D.}=V_{DB}=15V$ $V_{IN}=5V$, $I_C=20A,T_j=125°C$	-	2.05	-	V
V_f	FWDforward voltage	$V_{IN}=0V,I_C=-20A,T_j=25°C$		2.3	3.3	μs
t_{ON}	Switching time (remark2)	$V_{CC}=300V,V_{D.}=V_{DB}=15V$ $I_C=10A$ $V_{IN}=0V-5V$,Inductive load	-	0.75	-	μs
$t_{C(ON)}$			-	0.12	-	μs
t_{OFF}			-	0.9	-	μs
$t_{C(OFF)}$			-	0.08	-	μs
t_{rr}			-	0.18	-	μs
$E_{.on}$	turn-on loss	$I_C=10A$, Vcc=400V, $V_{D.}=V_{DB}=15V$ $R_G=47Ω$,L=1mH,$L_{the\ s}$=150nH, Tj=25°C		114	168	μJ
$E_{.off}$	Turn off loss			420	486	μJ
I_{CES}	Collector to Emitter Leakage Current	$V_{CE}=V_{CES}$Tj=25°C	-	-	75	μA
		$V_{CE}=V_{CES}$Tj=125°C		-	1	mA

Remark2:tONandtOFFincluding driverICInternal transmission delay time.tC(ON)andtC(OFF)yesIGBTIt is the switching time under the internally given gate drive conditions. See picture for details4.



(a)turn on (b)turn off

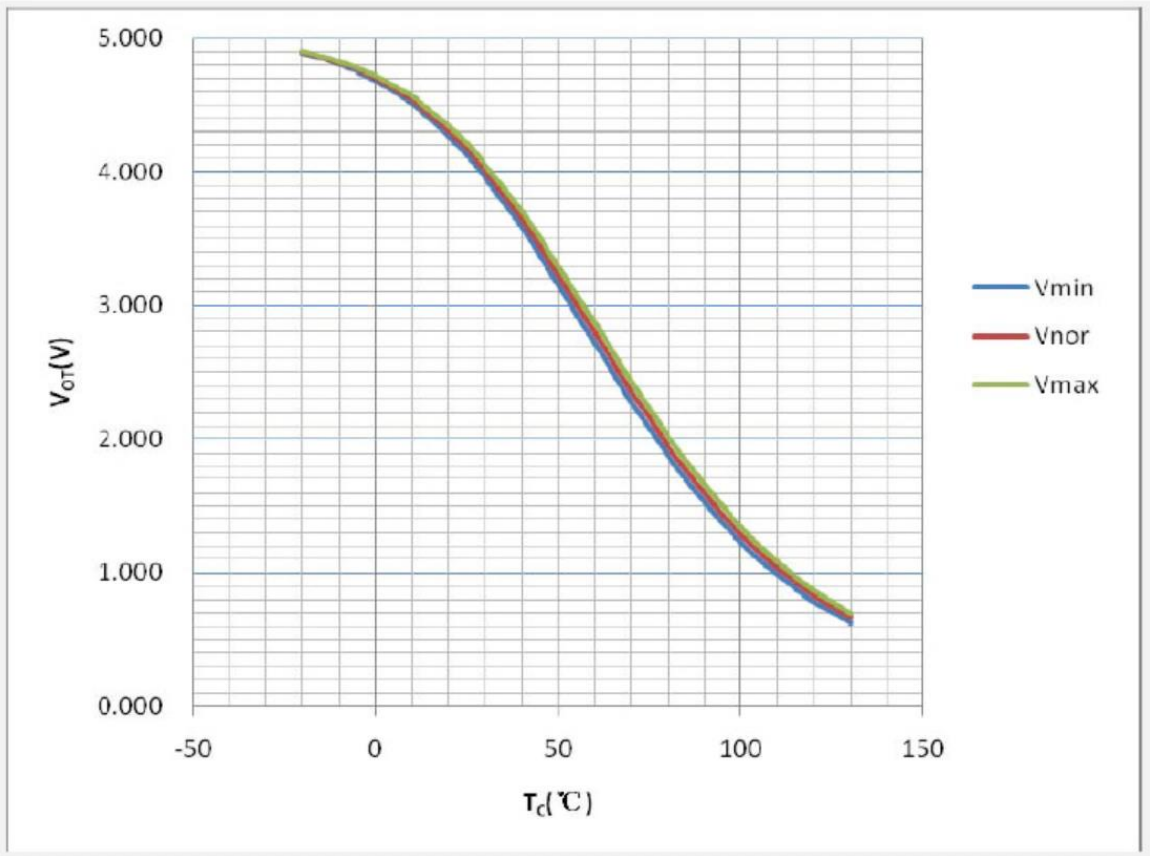
picture4: Switching time definition

Control section

mark	project	condition		minimum value	typical value	maximum value	unit
ID.	VD.Quiescent Current	VD.=15V VIN=5V	VP1-VNC	-	0.52	1	mA
IDB	VDBQuiescent Current	VDB=15V VIN=5V	UFB-U, VFB-V, WFB-W	-	360	550	uA
VFOH	Fault output voltage	Vsc=0V,FOfeet through10KResistor pull up to 5V		4.6	-	-	V
VFOL		Vsc=1V, IFO=1.5mA		-	-	0.3	V
Vsc,TH+	Short circuit forward trigger threshold	VD.=15V		0.37	0.47	0.65	V
Vsc,TH-	Short circuit negative trigger threshold	VD.=15V		0.2	0.4	-	V
UVDR	Power supply undervoltage protection control	reset level		11.0	12.1	12.8	V
UVDD		trigger level		9.5	10.4	11	V
UVDBR		reset level		11.0	12.1	12.8	V
UVDBD		trigger level		9.5	10.4	11	V
Ron, FLT	Fault Low Effective Impedance	I=1.5mA			50	90	Ω
TFO	Fault output pulse width			40	65	100	u
tFIL,IN	Input signal filter time (UP/VP/WP,UN/VN/WN)	VIN=0V&5V		140	290	-	wxya
tCINMIN	CINInput signal filter time	VIN=0V&5V,VCIN=5V		270	530	780	wxya

$V_{IN\ (ON)}$	Turn on threshold voltage	apply toUP,VP,WP,UN,VN,WNand VNCbetween	1.7	2.1	2.4	V
$V_{IN\ (OFF)}$	Turn-off Threshold Voltage		0.7	0.85	1.3	V
V_{OT}	temperature output, note3	Tc=90°C	1.53	1.59	1.65	V
		Tc=25°C	4.15	4.17	4.19	V
V_f	BSDForward Voltage	I_F=10mAIncluding voltage	-	1.0	1.3	V
R_{BSD}	BSDCurrent limiting resistor	VF1=4V, VF2=5V	twenty two	36	50	Ω

Remark3:When the temperature reaches the limit,IPMCan't close automaticallyIGBTand output fault signal. When the temperature exceeds the limit value defined by the user, the controller should be used (single chip) offIPM.IPMofVOTPlease refer to the figure for the output characteristic curve5,picture5The curve is based on20KPull-up resistor test result.



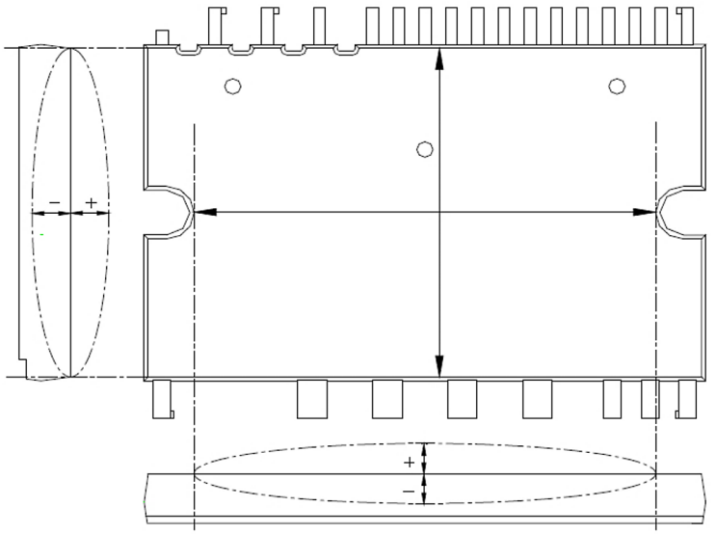
picture5:VOTOutput voltage curve

Recommended working conditions

mark	project	condition	value			unit
			minimum value	typical value	maximum value	
V_{CC}	voltage	apply toP–NU,NV,NWbetween	0	300	400	V
$V_{D.}$	Control supply voltage	apply toVP1–VNCbetween	-	15	-	V
V_{DS}	Upper arm control supply voltage	apply toVUFB–U,VVFB–V, VWFB-Wbetween	-	15	-	V
t_{dead}	dead time	The input of each bridge arm corresponds to,Tc<=100°C	1	-	-	us
f_{PWM}	PWMfrequency	- 20°C≤Tc≤+100°C - 20°C≤Tj≤+150°C	-	-	20	kHz
PWM	Minimum input signal pulse width	ON	0.7	-	-	us
		OFF	0.7	-	-	us
Tj	junction temperature		- 20	-	125	°C
internalNTC –Thermal resistance characteristics						
R_{NTC}	Thermistor	T_{NTC}=25°C	97	100	103	KΩ
		T_{NTC}=125°C	3.25	3.46	3.69	KΩ
temperature range			- 40	-	- 40	°C

mechanical properties

parameter	condition	value			unit
		minimum value	typical value	maximum value	
Mounting torque	Screw size:M3	-	0.69	-	N·m
Design flatness	see picture6	- 50	-	+ 120	um
weight		-	7	-	g



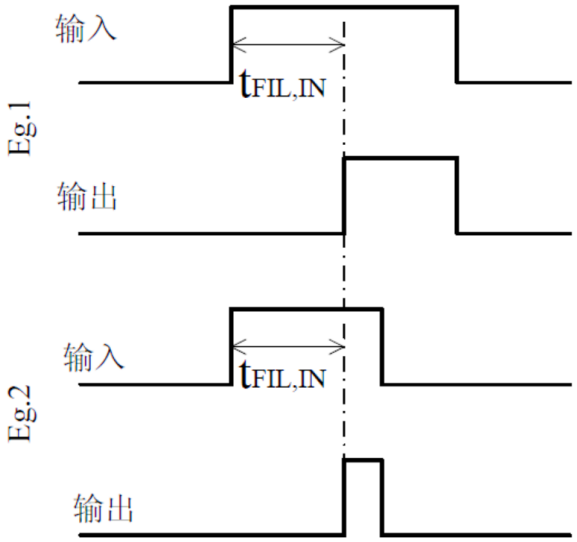
picture6: Flatness detection position

Application Guide

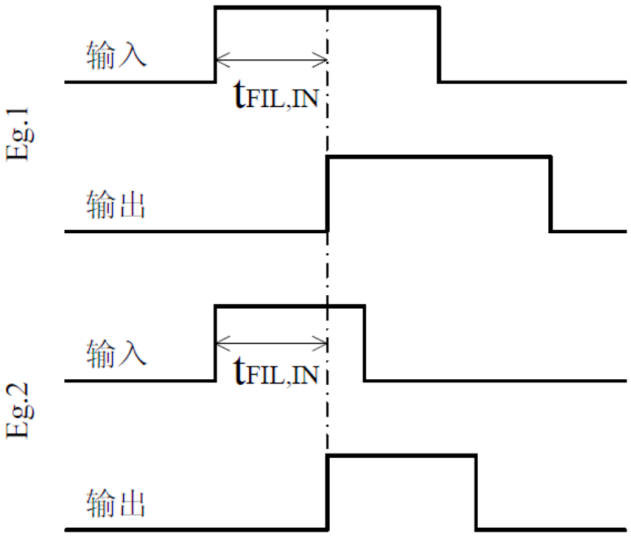
Enhanced Input Filtering

Enhanced filters improve theHVICThe consistency of the input/output pulses of the internal modules helps to filter out peak interference signals and narrow pulses, as shown in the figure below7 and diagram8

It is a demonstration diagram of the classic input filter and the enhanced input filter.

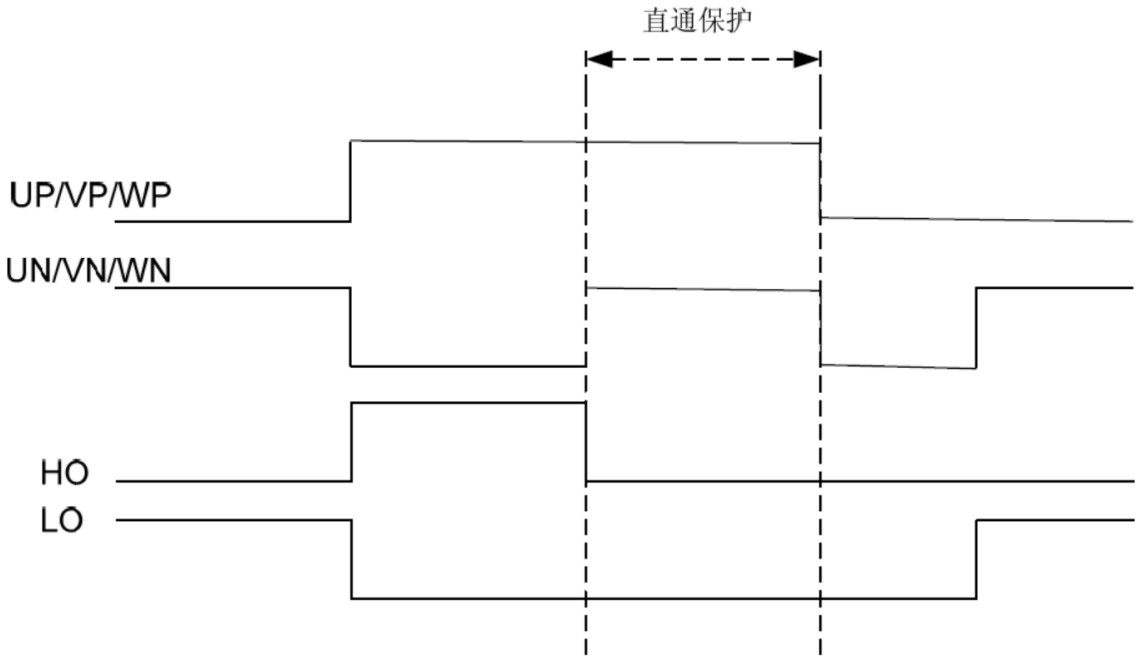


picture7: Typical Input Filtering



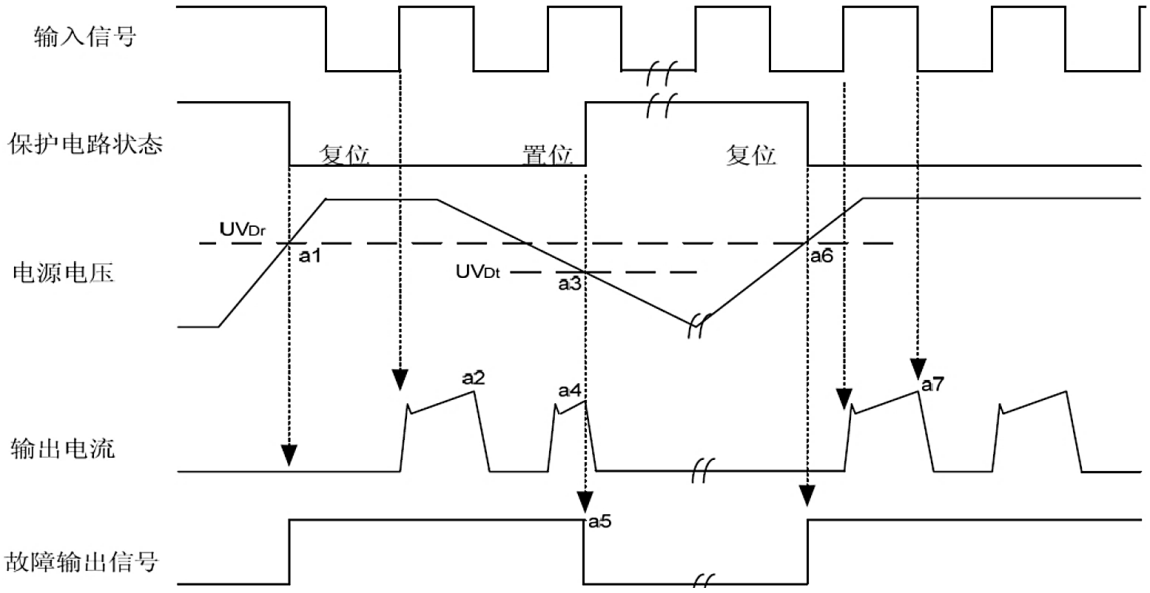
picture8: Enhanced input filtering

Protection Function Timing Diagram



picture9: cut-through protection

Remark4:HOandLOfor internalHVICGate output signal.



picture10:Timing Diagram of Undervoltage Protection (Low Side)

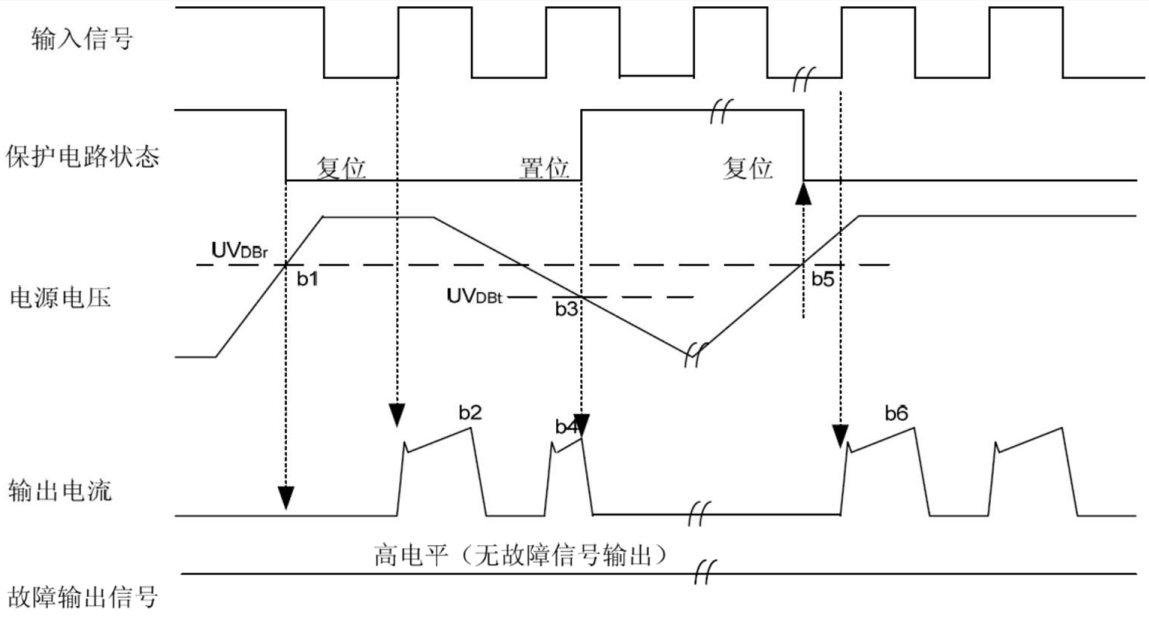
a1 :Power supply voltage rise: When the voltage rises to the undervoltage recovery point, the circuit will start running before the next undervoltage signal is executed. a2:normal operation:IGBTTurn on and apply current. a3:Undervoltage detection point (UV_{Dt}).

a4 :Regardless of the input signal,IGBTAll are closed. a5 :

The fault output is on.

a6 :Brown-out recovery ($UV_{Dr.}$).

a7 :normal operation:IGBTturns on and loads the load current.



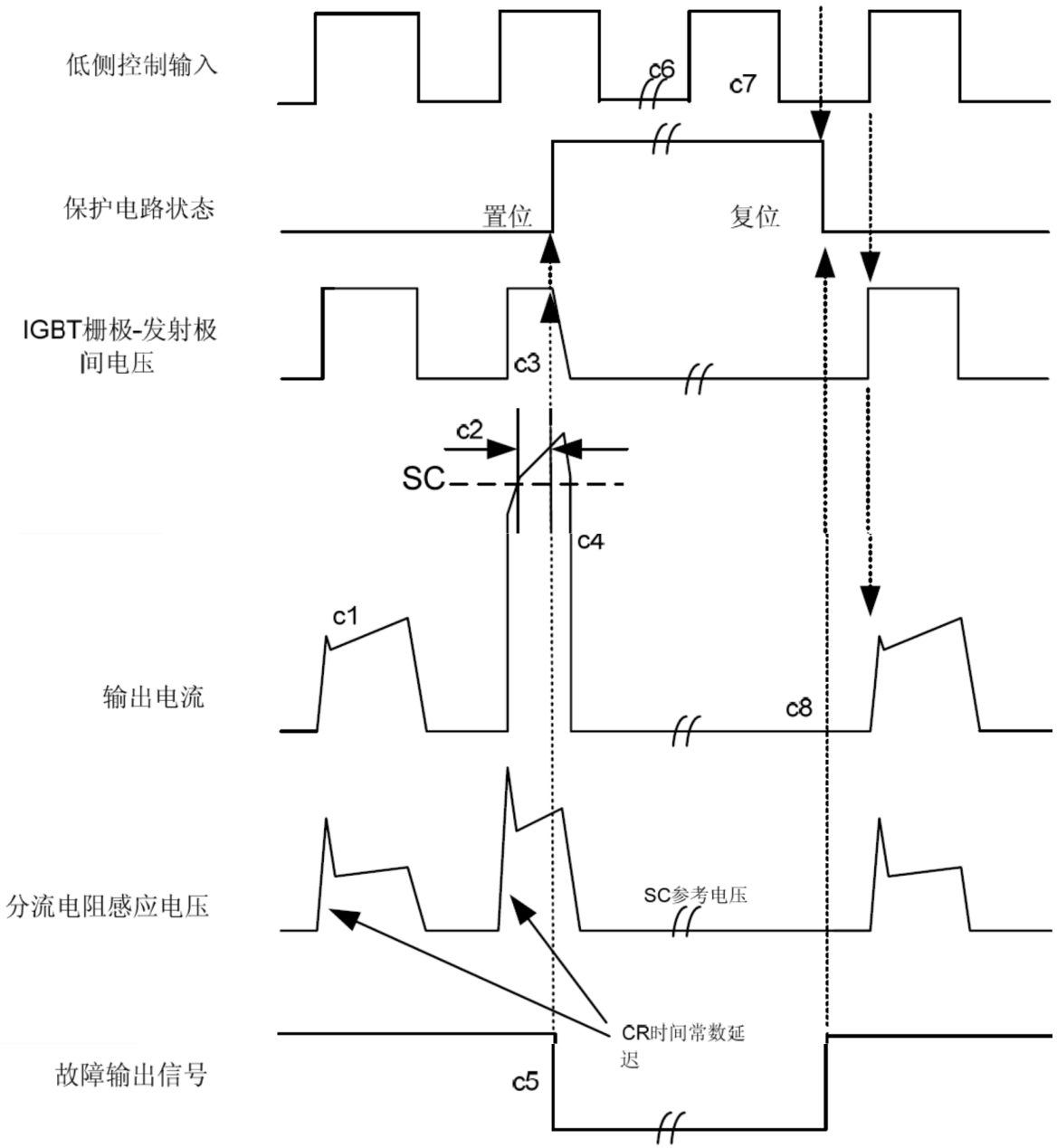
picture11:Timing Diagram of Undervoltage Protection (High Side)

b1:Power supply voltage rise: When the voltage rises to the undervoltage recovery point, the circuit will start running before the next undervoltage signal is executed. b2:normal operation:IGBTturns on and loads the load current. b3:Brown-out detection (UV_{DBt}).

b4:Regardless of the input signal,IGBTAll are closed. b5 :

Brown-out recovery (UV_{DBr}).

b6:normal operation:IGBTturns on and loads the load current.



picture12:Timing diagram of short-circuit current protection (only for low side)

(connected via external shunt resistor)

c1:normal operation:IGBTConduction carries

current. c2:Short circuit current detection (CIN

trigger). c3: IGBTThe gate is forced to turn off.

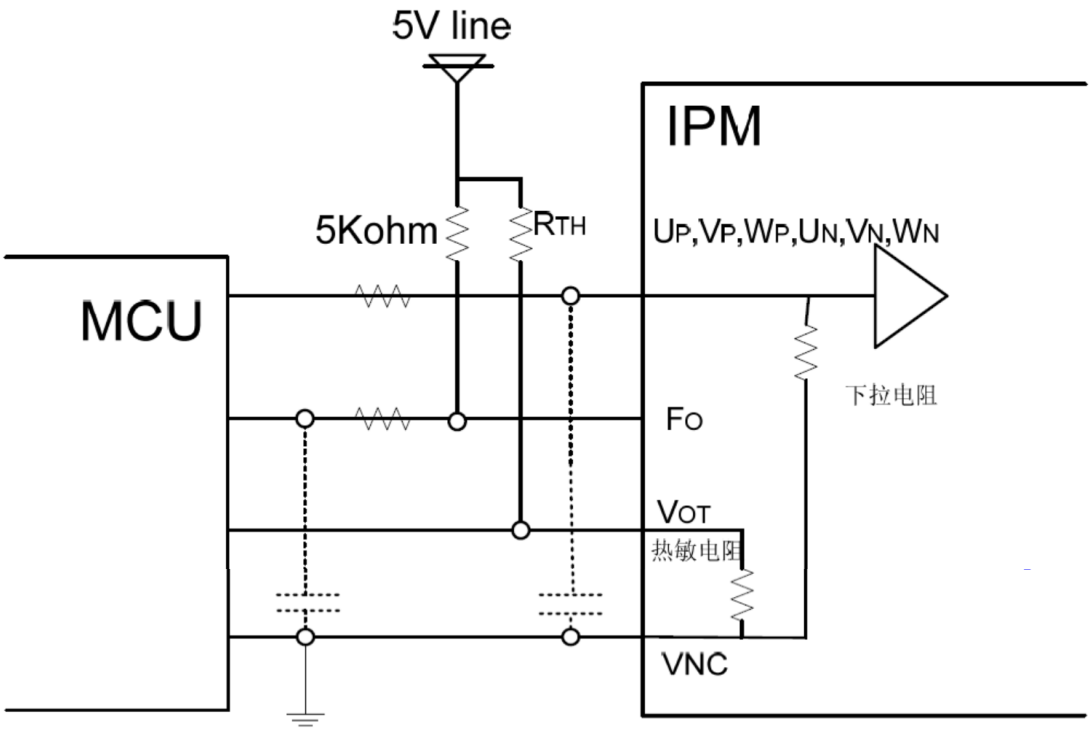
c4: IGBToff.

c5:The fault output timer starts running: the pulse width of the fault output signal is determined by the external capacitorCFO

set up. c6:enter"L" : IGBTclosure.

c7:enter"H": IGBTopen, but during fault signal action,IGBTNot conducting. c8 : IGBToff.

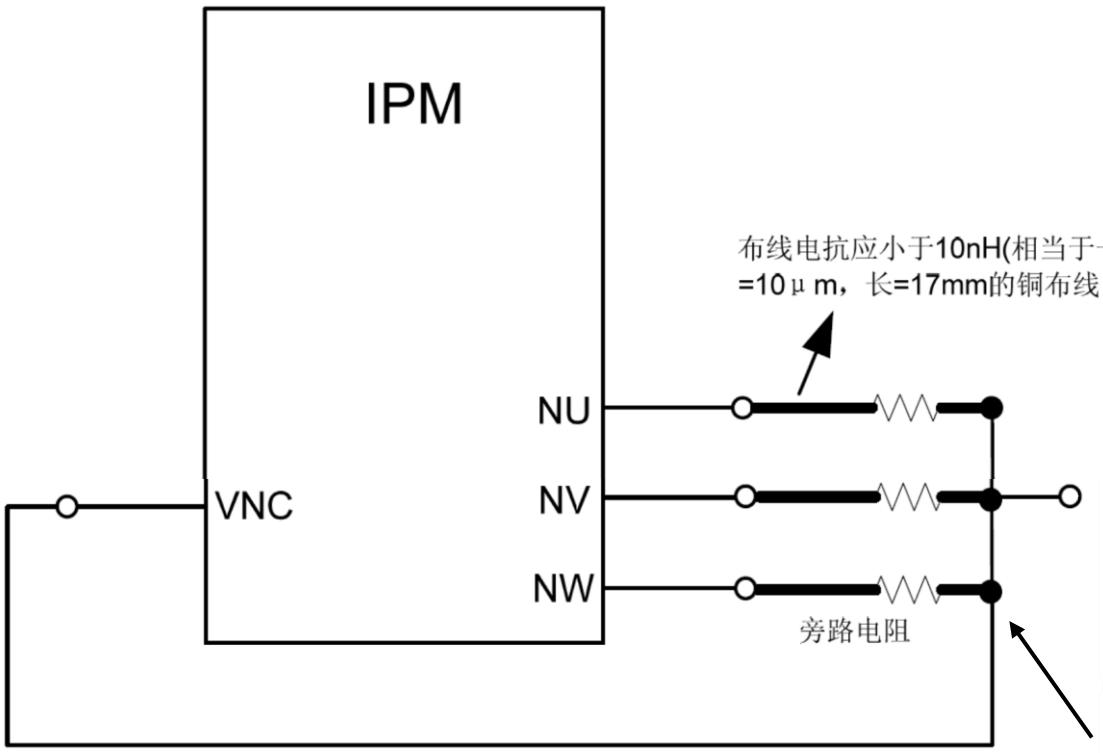
Input/Output Interface Circuit



picture13:recommendedMCUInput and output interface circuit

Remark5:becausePWMThe control method and the impedance of the actual application circuit and the impedance of the circuit board,RCDecoupling may vary. Remark6:Logic inputs are to be combined with standardCMOSorLSTTLThe output matches.

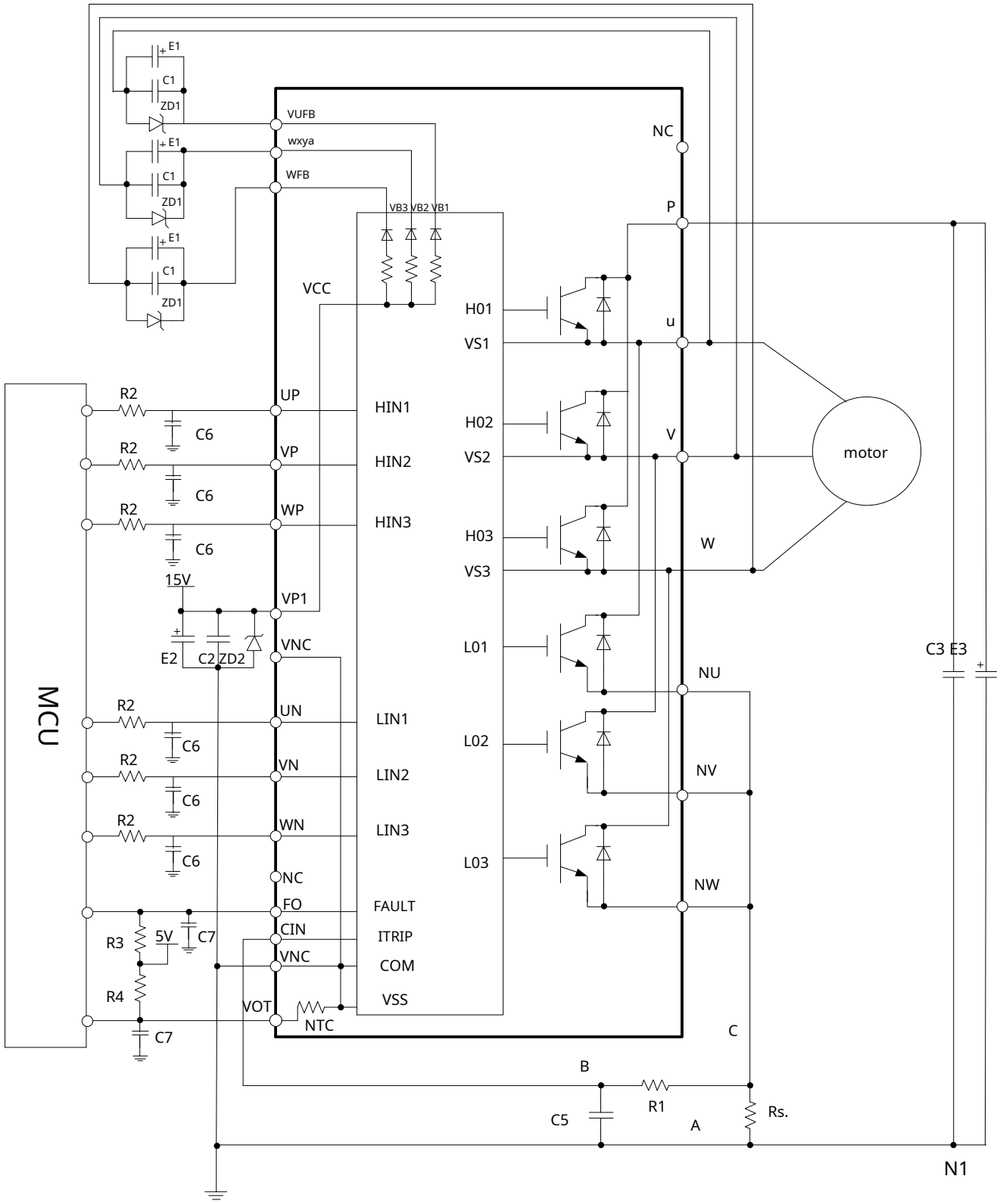
Shunt Resistor Wiring



picture14:Precautions for bypass resistor wiring

The connection between the shunt resistor and the control ground should be short amount

Typical application circuit diagram



picture15:Typical Application Circuit

Remark7:Input drive active high;ICIntegrates a5kΩ(typical value) pull-down resistor; in order to prevent malfunction, the input wiring should be as short as possible; when using

RCWhen decoupling lines, ensure that the input signal reaches the turn-on and turn-off threshold voltage range.

Remark8:Since the module has built-in dedicatedHVIC,Its control terminals can be connected withCPUThe terminals are directly connected without any isolation circuit such as optocoupler or transformer. Remark9:The negative terminal of the bootstrap circuit should be connected directly to theu,V,Wend.

Remark10:FOIt is an open-drain type, and its signal line should pass through a10kΩThe pull-up resistor pulls up to +5V/3.3Vpower supply. Remark11:In order to prevent false protection,A,B,CWires should be as short as possible.

Remark12:protection lineR1,C5The time constant is recommended to be selected in1~2uS. The off time may vary somewhat depending on the wiring. suggestionR1, C5Select Small Tolerance, Temperature Compensation Type.

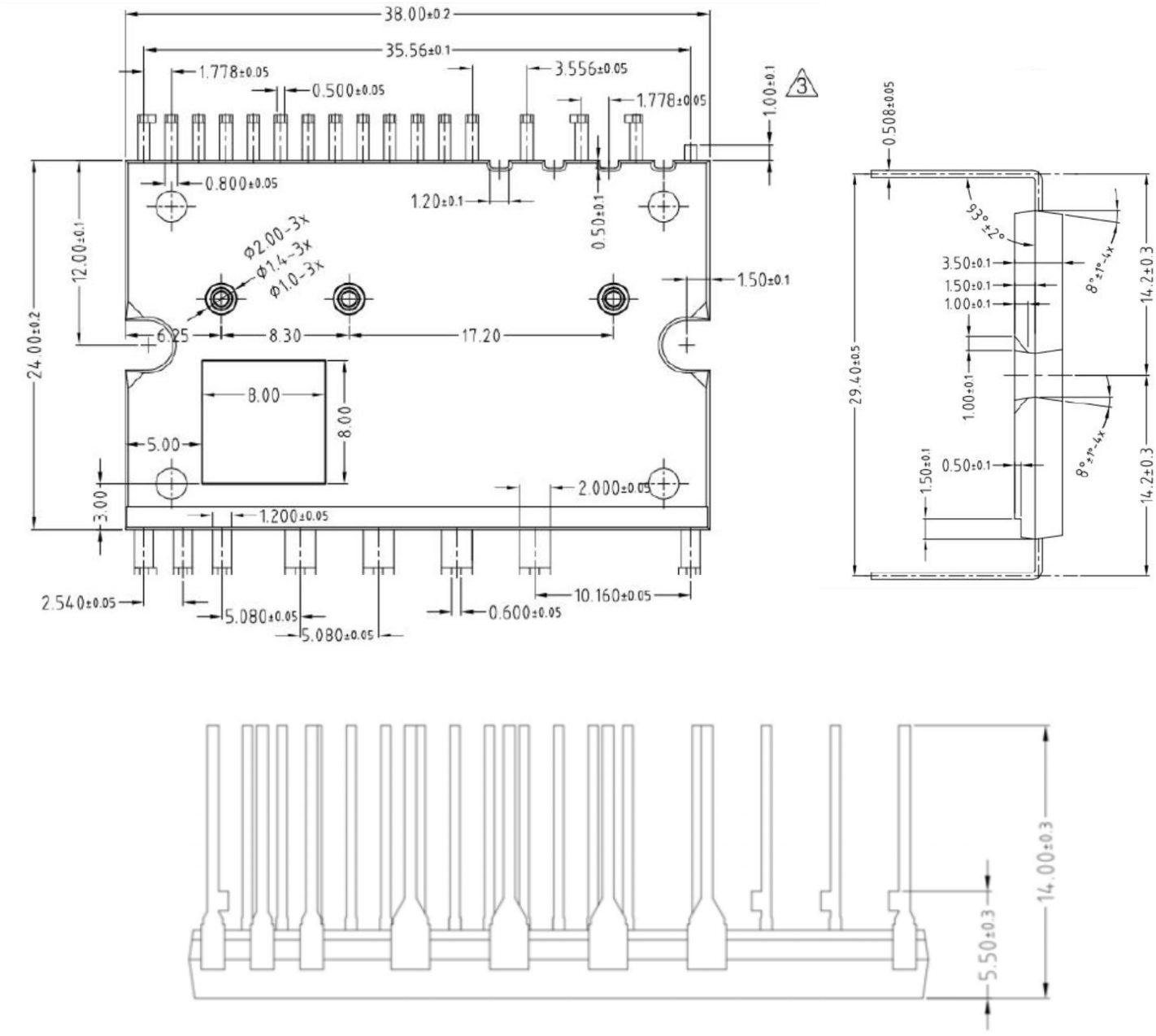
Remark13:All capacitors are located as close as possible toIPM.

Remark14:In order to prevent noise interference, the energy storage capacitor andP&N1The leads between theP&N1Approx. between terminals0.1~0.22uFof MLCCLow frequency filter capacitor.

Remark15:twoVNCend(9&16feet) inIPMInternally connected together, externally eitherVNCterminal connected toGND,The other terminal allows an open circuit. Remark16:if controlled byPCB The wiring is connected to the power ground, and the control signal may be affected by the fluctuation of the power ground. It is recommended to use a single point connection.

Outline package drawing

unit:mm



picture16:Package Outline Drawing